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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-2149

First Inventor or Application Identifier: Hisashi OHTANI et al.

Title: METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [32]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [2]
4. [X] Oath or Declaration *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed)
      [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

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6. [ ] Microfiche Computer Program *(Appendix)*

7 Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement [ ] Copies of IDS Citations (IDS)/PTO-1449
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity [ ] Statement filed in prior application, Statement(s) Status still proper and desired (PTO/SB/09-12)
15. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. [X] Other: Notice of Change of Company Name and Address

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
Divisional of prior application Serial No. 08/861,001 filed May 21, 1997; which itself is a Continuation of Application Serial No. 08/347,247 filed November 23, 1994, abandoned.
Prior application information: Examiner: M. Lebentritt Group/Art Unit: 2824

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label Customer No 22204 or [X] Correspondence address below

(Insert Customer No or Attach bar code label here)

Name. Eric J Robinson
Firm: NIXON PEABODY LLP
Address: 8180 Greensboro Drive, Suite 800
City: McLean State: VA Zip Code. 22102
Country: U.S.A. Telephone (703) 790-9110 FAX (703) 883-0370

Name: Eric J. Robinson Registration No. 38,285

Signature Date: June 14, 2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Hisashi OHTANI et al.	)
Based On Serial No. 08/861,001	) Art Unit: 2824
Which Was Filed: May 21, 1997	) Examiner: M. Lebentritt
For: METHOD FOR MANUFACTURING	)
A SEMICONDUCTOR DEVICE	) Date: June 14, 2000

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 08/861,001 filed May 21, 1997; which itself is a Continuation of Application Serial No. 08/347,247 filed November 23, 1994, abandoned.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. INDUSTRIAL FIELD OF APPLICATION

The present invention relates to a semiconductor device using crystalline semiconductor, and to a method for fabricating the same.

2. DISCUSSION OF PRIOR ART

Thin film transistors (referred to simply hereinafter as "TFTs") are well known as devices utilizing thin film semiconductors. The TFTs are fabricated by forming a thin film semiconductor on a substrate and processing the thin film semiconductor thereafter. The TFTs are widely used in various types of integrated circuits, and are particularly noticed in the field of switching elements that are provided to each of the pixels of active matrix liquid crystal display devices as well as in driver elements of the peripheral circuits thereof.

Amorphous silicon films can be utilized most readily as the thin film semiconductors for TFTS. However, an amorphous silicon film has a problem that the electrical characteristics thereof are inferior. This problem can be circumvented by using a thin film of crystalline silicon. Crystalline silicon film is also denoted as, for example, polycrystalline silicon, polysilicon and microcrystalline silicon. A thin film of crystalline silicon can be prepared by first forming a thin film of amorphous silicon, and then crystallizing it by heat treatment.

The heat treatment for the crystallization of the amorphous silicon film requires heating the film at a temperature of 600°C or higher for a

duration of 10 hours or longer. Such a heat treatment has a problem that a glass substrate cannot be used. For instance, a Corning 7059 glass commonly used for the substrate of an active matrix liquid crystal display device has a glass distortion point of 593°C, and is therefore not suitable for large area substrates that are subjected to heating at a temperature of 600°C or higher.

SUMMARY OF THE INVENTION

According to the study of the present inventors, it is found that the crystallization of an amorphous silicon film can be effected by heating the film at 550°C for a duration of about 4 hours. This can be accomplished by first introducing a trace amount of nickel or palladium, or other elements such as lead, into the surface of the amorphous silicon film.

The elements above (catalyst elements capable of accelerating the crystallization of an amorphous silicon film) can be introduced into the surface of the amorphous silicon film by plasma treatment or vapor deposition, or by ion implantation. The plasma treatment is a method comprising adding the catalyst elements onto the amorphous silicon film by generating a plasma of an atmosphere such as gaseous nitrogen or gaseous hydrogen in a plasma CVD apparatus of a parallel plate type or of a positive column type, while using a material containing catalyst elements as an electrode.

However, the presence of the catalyst elements in a large quantity in the semiconductor is not preferred, because the use of such semiconductors greatly impairs the reliability and the electric stability of the device in which the semiconductor is used. That is, the elements such as nickel which accelerate the crystallization (catalyst elements) are necessary in the crystallization of the amorphous silicon film, but are

preferably not incorporated in the crystallized silicon. These objects can be accomplished by selecting an element which tends to be inactive in crystalline silicon as the catalyst element, and by incorporating the catalyst element at a minimized amount for the crystallization of the film. Accordingly, the quantity of the catalyst element to be incorporated in the film must be controlled with high precision.

Also, in case of using nickel as the catalyst element, a crystalline silicon film was fabricated from an amorphous silicon film by adding nickel by plasma treatment, and the crystallization process and the like was studied in detail to obtain the following findings as a result:

(1) In case of incorporating nickel by plasma treatment into an amorphous silicon film, nickel is found to intrude into the film to a considerable depth of the amorphous silicon film before subjecting the film to heat treatment.

(2) The initial nucleation occurs from the surface from which nickel is incorporated.

(3) When a nickel layer is deposited on the amorphous silicon film by vapor deposition, the crystallization of an amorphous silicon film occurs in the same manner as in the case of effecting plasma treatment.

It can be concluded from the above findings that not all of nickel atoms incorporated by plasma treatment into the amorphous silicon film function effectively, and that, more importantly, only a trace amount of nickel need to be incorporated in the vicinity of the surface of the amorphous silicon film. Assumably, a point (or a plane) at which silicon is brought into contact with nickel contributes to the low temperature crystallization of amorphous silicon. Conclusively, nickel atoms are preferably dispersed as finely as possible to accelerate the crystallization reaction. In other words, "nickel atoms need to be introduced in the

vicinity of the surface of amorphous silicon film at a minimum concentration necessary for the low temperature crystallization of the amorphous silicon film".

A trace amount of nickel, i.e., a catalyst element capable of accelerating the crystallization of the amorphous silicon, can be incorporated in the vicinity of the surface of the amorphous silicon film by, for example, vapor deposition. However, vapor deposition is disadvantageous concerning the controllability of the film, and is therefore not suitable for controlling precisely the amount of the catalyst element that is incorporated in the amorphous silicon film.

In particular, the crystals can be grown in parallel with the plane of catalyst element the silicon film from the region onto which the solution is applied to the region onto which the solution is not applied. It is also confirmed that this region of crystal growth contains the catalyst element at a low concentration and that it is extremely useful to utilize such a crystalline silicon film as an active layer region for a semiconductor device. However, there remains a problem how to selectively introduce the catalyst elements.

An object of the present invention is to provide a method for fabricating a thin film semiconductor of crystalline silicon, characterized in that it satisfies the following requirements:

(1) The catalyst element is introduced at a controlled and at a minimum possible quantity;

(2) The catalyst element is introduced into selected portions; and

(3) The process yields high productivity.

The present invention uses the following means to accomplish the object above. Specifically, a mask-patterned amorphous silicon film is crystallized by bringing it into contact with either a pure catalyst element

which accelerates the crystallization of the amorphous silicon film or a compound containing the catalyst element, while applying heat treatment thereto.

More specifically, a solution containing the catalyst element is applied to the surface of an amorphous silicon film having a desired pattern formed thereon using a resist. In this manner, the catalyst element is introduced into the surface of the amorphous silicon film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a method of the present invention.

Fig. 2 shows a process of fabrication of an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is characterized in that the catalyst element is introduced by bringing it into contact with the surface of the amorphous silicon film having a pattern formed thereon by using a resist.

The present invention is also characterized in that the thin film crystalline silicon thus crystallized using the catalyst element is employed in the constitution of an active region having at least one of the electric junctions such as a PN, a PI, and an NI junction of the semiconductor device. Specifically mentioned as the semiconductor devices are a thin film transistor (TFT), a diode, and an optical sensor.

The present invention are basically advantageous in the following aspects:

(a) The concentration of the catalyst element in the solution can be strictly controlled to a minimum and optimum value suitable for increasing the crystallinity of the thin film silicon;

(b) The quantity of the catalyst element introduced in the amorphous silicon film can be controlled by adjusting the concentration of the catalyst element in the solution so long as the solution is brought into contact with the surface of the amorphous silicon film;

(c) The catalyst element can be introduced into the amorphous silicon film at an amount as low as possible, because the catalyst element adsorbed by the surface of the amorphous silicon film principally contributes to the crystallization of silicon; and

(d) The catalyst element can be selectively introduced into the surface of the amorphous silicon film by using a resist pattern; thus, a semiconductor device utilizing the region crystallized alone the transverse direction can be easily fabricated.

The solution containing a catalyst element for accelerating the crystallization can be applied to the surface of the amorphous silicon film by using, for example, an aqueous solution or a solution based on an organic solvent. The "solution" as referred herein encompasses those containing the catalyst element in the form of a compound dissolved in the solution, and those containing the element in the form of a dispersion. Preferably the kind of the solution is selected by taking the affinity of the solvent with the catalyst element into consideration. It is also preferred to consider the contact angle of the solution and the surface of the thin film in selecting the solution. When a fine pattern is formed, in particular, a material having a small contact angle is preferably used to process the amorphous silicon film deeply into the pattern.

The solvent containing the catalyst element may be selected from various types of polar solvents such as water, an alcohol, an acid, or ammonia.

When nickel is used as the catalyst, it may be added in a polar solvent in the form of a nickel compound. More specifically, it may be selected from a group of representative nickel compounds, i.e., nickel bromide, nickel acetate, nickel oxalate, nickel carbonate, nickel chloride, nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetylacetonate, nickel 4-cyclohexylbutyrate, nickel oxide, and nickel hydroxide.

Otherwise, a non-polar solvent can be used in the solution containing the catalyst element. For example, a solvent selected from benzene, toluene, xylene, carbon tetrachloride, chloroform, ether, trichloroethylene, and Freon can be used as well. It should be noted, however, that "polarity" is referred herein not in a strict sense considering dipole moment, but in a general sense based on chemical characteristics.

In this case, nickel is incorporated in the solution in the form of a nickel compound. Representative compounds to be mentioned include nickel acetylacetonate and nickel 2-ethylhexanoate.

It is also useful to add a surface active agent into the solution containing the catalyst element. The surfactant increases the adhesion strength of the solution and controls the adsorptivity. The surfactant may be applied previously to the surface of the substrate onto which the amorphous silicon is deposited.

When metallic nickel is used as the catalyst, it may be dissolved into an acid to provide a solution.

The description above is for a case nickel is dissolved completely in a solution. Nickel need not be completely dissolved in a solution, and

other materials, such as an emulsion comprising metallic nickel or a nickel compound in the form of a powder dispersed in a dispersant may be used as well.

The same as those mentioned in the foregoing applies to the case in which a catalyst element other than nickel is used.

When nickel is used as the catalyst element for accelerating the crystallization of amorphous silicon, it may be incorporated in a polar solvent such as water. However, on applying the solution to a thin film of amorphous silicon directly, the solution is sometimes found to be repelled by the surface of the amorphous silicon. This can be circumvented by forming a thin oxide film 100 Å or less in thickness, and then applying a solution containing the catalyst element thereon. In this manner, a uniform coating can be formed on the surface of amorphous silicon. It is also useful to improve the wettability of the amorphous silicon with the solution by adding a surfactant and the like into the solution.

A solution can be directly applied to the surface of an amorphous silicon film by using a non-polar solvent such as toluene. For instance, a toluene solution of nickel 2-ethylhexanoate can be used favorably in such a case. It is also effective in this case to previously apply an adhesive or a like material commonly used in the case of forming, a resist coating However, such an agent must be treated with care lest it should be applied to an excessive amount, because the presence of the additive in excess obstructs the addition of a catalyst element inside amorphous silicon.

The concentration of the catalyst element in the solution depends on the kind of the solution, however, roughly speaking, the concentration of nickel by weight is from 1 ppm to 200 ppm, and preferably, from 1 ppm to 50 ppm. The concentration is determined based on the nickel

concentration or the resistance against hydrofluoric acid of the film upon completion of the crystallization.

The crystal growth can be controlled by applying the solution containing the catalyst element to the selected portions of the amorphous silicon film. In particular, the crystals can be grown in parallel with the plane of the silicon film from the region onto which the solution is applied to the region onto which the solution is not applied. The region in which the crystals are grown in parallel with the plane of the amorphous silicon film is referred to as the region crystallized in the lateral direction.

It is also confirmed that this region crystallized in the lateral direction contains the catalyst element at a low concentration. It is useful to utilize a crystalline silicon film as an active layer region for a semiconductor device, however, in general, the concentration of the impurity in the active region is preferably as low as possible. Accordingly, the use of the region crystallized in the lateral direction for the active layer region is useful in fabricating a device.

The use of nickel as the catalyst element is particularly effective in the method according to the present invention. However, other useful catalyst elements can be used as well. Such catalyst elements include Ni, Pd, Pt, Cu, Aa, Au, In, Sn, Pd, Sn, Pd, P, As, and Sb. Otherwise, the catalyst element may be at least one selected from the elements belonging to the Group VIII, IIIB, IVb, and Vb of the periodic table. When iron (Fe) is selected as the catalyst element, an iron salt selected from compounds such as ferrous bromide ($FeBr_2 \cdot 6H_2O$), ferric bromide ($FeBr_3 \cdot 6H_2O$), ferric acetate ($Fe(C_2)H_3O_2)_3 \cdot xH_2O$), ferrous chloride ($FeCl_2 \cdot 4H_20$), ferric chloride ($FeCl_3 \cdot 6H_2O$), ferric fluoride ($FeF_3 \cdot 3H_2O$), ferric nitrate ($Fe(NO_3)_3 \cdot 9H_20$), ferrous phosphate ($Fe(PO_4)2 \cdot 8H_20$), and ferric phosphate ($FePO_4 \cdot 2H_20$) can be used.

In case cobalt (Co) is used as the catalyst element, useful compounds thereof include cobalt salts such as cobalt bromide ($CoBr \cdot 6H_2O$), cobalt acetate ($Co(C_2H_3O_2)_2 \cdot 4H_2O$), cobalt chloride ($CoCl_2 \cdot 6H_2O$), cobalt fluoride ($CoF_2 \cdot xH_2O$), and cobalt nitrate ($Co(NO_3)_2 \cdot 6H_2O$).

A compound of ruthenium (Ru) can be used in the form of a ruthenium salt, such as ruthenium chloride ($RuCl_3 \cdot H_20$).

A rhodium (Rh) compound is also usable in the form of a rhodium salt, such as rhodium chloride ($RhCl_3 \cdot 3H_2O$).

A palladium (Pd) compound is also useful in the form of a palladium salt, such as palladium chloride ($PdCl_2 \cdot 2H_2O$).

In case osmium (Os) is selected as the catalyst element, useful osmium compounds are osmium salts such as osmium chloride ($OsCl_3$).

If iridium (Ir) is selected as the catalyst element, a compound selected from iridium salts such as iridium trichloride ($IrCl_3 \cdot 3H_20$) and iridium tetrachloride ($IrCl_4$) can be used.

In case platinum (Pt) is used as the catalyst element, a platinum salt such as platinic chloride ($PtCl_4 \cdot 5H_2O$) can be used as the compound.

In case copper (Cu) is used as the catalyst element, a compound selected from cupric acetate ($Cu(CH_3COO)_2$), cupric chloride ($CuCl_2 \cdot 2H_20$), and cupric nitrate ($CU(NO_3)_2 \cdot 3H_20$) can be used.

In using gold (Au) as the catalyst element, it is incorporated in the form of a compound selected from auric trichloride ($AuCl_3 \cdot xH_20$), auric, chloride ($AuHCl_4 \cdot 4H_20$), and sodium auric tetrachloride ($AuNaCl_4 \cdot 2H_2O$).

The catalyst elements can be incorporated not only by using a solution such as an aqueous solution and an alcohol solution, but also by using a substance selected from a wide variety of materials containing the catalyst element. For instance, metal compounds and oxides containing the catalyst element can be used as well.

EXAMPLES

EXAMPLE 1

The present example refers to a method which comprises forming a desired mask pattern on the surface of an amorphous silicon film using a resist mask, and then introducing nickel into selected portions of the amorphous silicon film by applying a solution containing nickel to the surface of the amorphous silicon film having thereon the mask pattern.

Referring to Fig. 1, the method according to the present example is described below. First, a resist pattern 21 is formed as a mask on a glass substrate (a Corning 7059 class substrate, 100 mm x 100 mm). Either a positive or a negative resist can be used.

The resist mask 21 is patterned as desired by means of an ordinary patterning process using photolithography. A thin silicon oxide film 20 is deposited thereafter by irradiating an ultraviolet radiation in gaseous oxygen. The thin silicon oxide film 20 can be fabricated by irradiating the UV light for a duration of 5 minutes under gaseous oxygen. Assumably, a silicon oxide film 20 about 20 to 50 Å in thickness is obtained in this step (Fig. 1(A)).

The ultrathin silicon oxide film 20 thus obtained is provided for an aim to improve the wettability of amorphous silicon film 12 on applying thereto a nickel-containing solution in the later step. Instead of irradiating a UV light, the oxide film can be formed by immersing the substrate into aqueous hydrogen peroxide heated to 70°C for a duration of 5 minutes. A thermally oxidized film can be used as well.

After forming the oxide film, 5 ml (in case of a substrate 10 x 10 cm^2 in area) of an aqueous acetate solution containing nickel at a concentration of 100 ppm by weight is applied dropwise to the substrate.

After spincoating the surface of the substrate by operating a spinner at 50 rpm for a duration of 10 seconds to obtain a uniform aqueous coating on the entire surface, the substrate is maintained as it is for a duration of 5 minutes. Spin drying at 2,000 rpm is effected for 60 seconds thereafter. The retention of the aqueous coating on the surface of the substrate can be effected on a spinner, while rotating the substrate at a rate of 150 rpm or lower (Fig. 1(B)).

The resist mask 21 is removed thereafter by oxygen ashing to selectively form a region containing nickel adsorbed thereon. Instead of using oxygen ashing, the resist mask can be removed by annealing it in oxygen.

The amorphous silicon film 12 is crystallized thereafter by applying a heat treatment at 550°C (in gaseous nitrogen) for a duration of 4 hours. It is found that the crystal growth occurs from the region 22 into which nickel is incorporated, towards the region 23 in which nickel is not introduced. Referring to Fig. 1(C), nickel is directly introduced into the region 24. Upon crystallizing the region 24, it can be seen that the crystallization proceeds in the lateral direction to provide a region 25. It is confirmed that crystals in the crystallized region 25 grow approximately along the direction of the crystallographic <111> axis.

It is also useful to employ annealing after the step of crystallization. The annealing is effected by using a laser radiation or an intense light equivalent thereto. A thin film of crystalline silicon further improved in crystallinity can be obtained. A laser beam emitted from a KrF excimer laser or a XeCl laser can be used. An infrared radiation is also useful for the annealing. Annealing can be effectively carried out by using an infrared radiation, because infrared light is selectively absorbed by silicon and not by the glass substrate.

By controlling the concentration of the solution and the duration of retention of the solution on the surface of the amorphous silicon film, it is possible to control the concentration of nickel in the region of direct addition to a range of from 1 x 10^{16} atoms·cm^{-3} to 1 x 10^{19} atoms·cm^{-3}. At the same time, the concentration of nickel in the region of lateral crystal growth can be controlled to a range lower than that of the region above.

The crystalline silicon film thus obtained according to the method of the present example is characterized in that it yields an excellent resistance against hydrofluoric acid. This is in clear contrast with the case in which nickel is introduced by a plasma process, because in accordance with the findings of the present inventors, thin film crystalline silicon obtained by crystallizing an amorphous silicon film after introducing nickel by a plasma process is inferior with respect to the resistance against hydrofluoric acid.

For instance, the poor resistance against hydrofluoric acid is critical in case of providing an electrode by perforating a silicon oxide film deposited as a gate dielectric or an interlayer insulating film on the surface of the thin film crystalline silicon. In such a case, in general, the silicon oxide film is removed by using a buffered hydrofluoric acid. If a thin film crystalline silicon inferior in resistance against hydrofluoric acid is used, it is found extremely difficult to remove the silicon oxide film alone without causing, damage to the thin film crystalline silicon.

However, if a thin film crystalline silicon having a sufficiently high resistance against hydrofluoric acid is used, the silicon oxide film alone can be removed selectively by taking the advantage of the large difference (selectivity ratio) between the etching rate of the silicon oxide film and the thin film crystalline silicon.

As described in the foregoing, the region of lateral crystal growth yields a high crystallinity, and yet, is very low in the concentration of the

catalyst element. Accordingly, the use of this region for the active layer region is useful in fabricating a device. More specifically, the use of this region as a channel region of a thin film transistor is particularly useful.

EXAMPLE 2

The present example relates to a case in which a catalyst element, nickel, is incorporated into a non-aqueous solvent, alcohol, and is applied to the surface of an amorphous silicon film. In the present case, nickel is added into alcohol in the form of nickel acetylacetonate. The concentration of nickel is adjusted as desired. The process steps thereafter are the same as those described in Example 1.

The present example is described in further detail below. First of all, nickel acetylacetonate is prepared for use as the starting material. Nickel acetylacetonate is soluble to alcohol, and decomposes at a low temperature. Accordingly, it can be readily decomposed by the heat during the crystallization step.

Ethanol is used as the alcohol. Nickel acetylacetonate is added into ethanol at such a concentration that nickel should be present in the solution at a concentration of 100 ppm.

The resulting solution is applied to the surface of an amorphous silicon film having already thereon a desired resist pattern formed by using Photonese. Photonese is used specifically in this case because it does not dissolve into alcohol after it is baked at 300°C. The amorphous silicon film used in this case is a film 1,000 Å in thickness, which is deposited by means of plasma CVD on a 100 x 100-mm² area glass substrate having thereon a base silicon oxide film (2,000 Å in thickness).

A smaller amount of solution is necessary in this case as compared with the case using an aqueous solution as in Example 1. This is ascribed

to the fact that the contact angle of alcohol is smaller than that of water. Thus, 2 ml of the solution is added dropwise to an area of 100 x 100 mm^2.

The resulting state is retained for a duration of 5 minutes and dried thereafter using a spinner. Drying is effected by operating the spinner at 1.500 rpm for a duration of 1 minute. Nickel salt is decomposed by heating the dried substrate at 350°C for a duration of 60 minutes. Thus, in this manner, nickel as a catalyst element can be introduced into the amorphous silicon film by allowing it to diffuse into amorphous silicon film. The Photonese mask is removed thereafter by wet etching using hydrazine or by ashing. A crystalline silicon film can be obtained in this manner by carrying out the crystallization process at 550°C for a duration of 4 hours.

As a matter of course, similar to the case as described in Example 1, crystal growth occurs in the lateral direction from the region into which the catalyst element is introduced to the region into which no catalyst element is added. Thus, a region of crystalline silicon is obtained extending in the lateral direction.

EXAMPLE 3

The present example relates to a case in which nickel is introduced as the catalyst element into selected portions of an amorphous silicon film by forming an oxide film containing nickel on an amorphous silicon film having thereon a resist pattern.

In the present example, an OCD solution containing a catalyst element for accelerating the crystallization is used to form an oxide film containing the catalyst element on the amorphous silicon film, and the oxide film is crystallized thereafter by heating. The OCD solution as referred herein is Ohka Diffusion Source manufactured by Tokyo Ohka

Kogyo Co., Ltd., and it comprises an organic solvent dissolved therein a silicon compound and additives. The OCD solution is useful, because a silicon oxide film can be readily obtained by applying the solution to an object and baking it thereafter. Furthermore, a silicon oxide film containing impurities can be easily obtained by using this solution.

A Corning 7059 glass substrate 100 mm x 100 mm in area is used in the present example.

An amorphous silicon film from 100 to 1,500 Å in thickness is deposited by plasma CVD or LPCVD. More specifically in this case, an amorphous silicon film was deposited at a thickness of 1.000 Å.

The resulting substrate is subjected to a treatment using hydrofluoric acid to remove stains and natural oxide films, and a resist pattern is formed as desired. It should be noted that a resist material having a sufficiently high resistance against the organic solvent in the OCD solution is selected in this case.

An oxide film containing nickel as the catalyst element is formed thereafter. Referring to Fig. 1, the oxide film is formed in the manner described below on the portion indicated with numeral 14 corresponding to the solution referred in Example 1.

A solution containing 0.2% by weight Of SiO_2 and from 200 to 2,000 ppm of nickel is prepared by mixing an OCD solution, i.e., OCD Type 2 Si 59000 manufactured by Tokyo Ohka Kogyo Co., Ltd., with a methyl acetate solution containing dissolved therein nickel (II) acetylacetonate.

Then, 10 ml of the resulting solution is applied dropwise to the surface of amorphous silicon film. Spin coating is effected by operating a spinner at a rate of 2,000 rpm for a duration of 15 seconds. A silicon oxide film containing nickel is formed at a thickness of about 1,300 Å by

effecting, prebaking at 150°C for a duration of 30 minutes. The temperature of prebaking can be determined by taking the decomposition temperature of the nickel compound into consideration.

The resist is removed thereafter using a stripping solution. Then, the resulting structure is subjected to heat treatment at 550°C for a duration of 4 hours under gaseous nitrogen in a heating furnace. As a result, a crystalline thin film of silicon can be obtained on the substrate. At the same time, crystal growth occurs in the lateral direction from the region into which nickel is introduced towards the region into which no nickel is added.

The heat treatment above can be carried out at a temperature of 450°C or higher. If the heat treatment were to be effected at a lower temperature, the treatment must be effected for a longer duration. Such a long treatment unfavorably impairs the production efficiency. If heating at a temperature of 550°C were to be carried out, on the other hand, the problem of heat resistance of the glass substrate must be overcome.

The concentration of nickel in the OCD solution cannot be determined alone, and is determined in correlation with the concentration of SiO_2 in the solution. Furthermore, the concentration of nickel must be determined by taking other factors into consideration, because the amount of nickel which diffuses from the silicon oxide film obtained from the OCD solution into the thin film crystalline silicon differs depending on the temperature and the duration of heating.

EXAMPLE 4

The present example relates to a method for fabricating an electronic device by using a region obtained by introducing nickel into selected regions and then allowing crystal growth to occur in the lateral direction

(a direction in parallel with the surface of the substrate). The concentration of nickel in the active layer of the device can be further lowered by employing the constitution according to the present example. This constitution is extremely favorable from the viewpoint of electric stability and reliability of the device.

Nickel can be incorporated by any of the methods described in the foregoing Examples 1 to 3.

The present example relates to a method for fabricating a TFT for use in controlling pixels of an active matrix addressed device. Referring to Fig. 2, the method for fabricating the TFT according to the present example is described below. First, a substrate 201 is cleaned, and a base silicon oxide film 202 is deposited thereon at a thickness of 2,000 Å by means of plasma CVD using gaseous TEOS (tetraethoxysilane) and oxygen as the starting materials. Then, an intrinsic (I-type) amorphous silicon film 203 is deposited at a thickness of from 500 to 1,000 Å. For instance, an I-type amorphous silicon film 203 is formed at a thickness of 1,000 Å in this case. A resist mask 205 is formed thereafter. A region of exposed amorphous silicon is obtained in this manner.

Subsequently, a solution (specifically, an acetate solution) containing, nickel as the catalyst element for accelerating the crystallization is applied according to the method described in Example 1. The nickel concentration is 100 ppm. The details and the process steps are the same as those described in Example 1. This step of coating may otherwise be effected by either of the processes described in Examples 2 and 3.

The silicon film 303 is crystallized thereafter by effecting annealing at a temperature in the range of from 500 to 620°C, for example, at 550° C, for a duration of 4 hours. The crystallization initiates from the region 206, i.e., a region in which the silicon film is brought into contact with

nickel, and proceeds along a direction in parallel with the substrate as indicated with an arrow in the figure. It can be seen in the figure that region 204 is crystallized by directly introducing nickel, and that region 203 is crystallized in the lateral direction. The region 203 crystallized in the lateral direction is composed of crystals about 25 μm in size. Furthermore, it is confirmed that crystals in the crystallized region 203 grow approximately along the direction of the crystallographic <111> axis (Fig. 2 (A)).

The silicon oxide film 205 is removed thereafter. The oxide film formed on the surface of the region 206 is removed at the same time. After patterning the silicon film 204, an island-like active layer region 208 is formed by dry etching. Referring to Fig. 2 (A), the region 206 represents the region rich in nickel, because nickel is introduced directly therein. It is also confirmed that the front end of crystal growth contains nickel at a high concentration. Such regions contain nickel in a concentration higher than those in the intermediate regions. Accordingly, the method according to the present example is designed as such that the channel forming region in the active layer 208 does not overlap those regions containing nickel at high concentration.

The surface of the active layer (silicon film) 208 is oxidized to form a silicon oxide film 209. The silicon oxide film 209 is obtained by allowing the active layer 208 to stand in an atmosphere containing 100% by volume of water vapor under a pressure of 10 atoms and at a temperature in the range of from 500 to 600°C, representatively, at 550°C. Thus is obtained the silicon oxide film 209 at a thickness of 1,000 Å. By thus forming the silicon oxide film 209 by thermal oxidation, the entire substrate is maintained at 400°C under 100% gaseous ammonia at 1 atm.

The silicon oxide film 209 is subjected to nitriding by irradiating an infrared radiation having a peak intensity in a wavelength range of from 0.6 to 4 μm, more preferably, for example, in a range of from 0.8 to 1.4 μm for a duration of 30 to 180 seconds. The atmosphere under which the process is effected may contain from 0.1 to 10% of gaseous HCl.

Halogen lamp is used as the light source of the infrared radiation. The intensity of the infrared radiation is controlled as such that the temperature as monitored on a single crystal silicon wafer may fall in a range of from 900 to 1,200°C. More specifically, the temperature is monitored on the silicon wafer using a thermocouple buried in the wafer, and the detected value is fed back to the light source. In the present example, the temperature is elevated at a constant rate in a range of from 50 to 200°C/sec, and is allowed to cool naturally at 20 to 100°C/sec. The method using infrared radiation is preferred, because infrared radiation selectively heats the silicon film. Thus, the heat effect to the glass substrate is minimized (Fig. 2 (B)).

Subsequently, an aluminum film is deposited at a thickness in a range of from 3,000 to 8,000 Å by sputtering. For instance, a 6,000 Å thick aluminum (containing from 0.01 to 0.2% of scandium) is deposited. The aluminum film thus obtained is patterned to obtain a gate electrode 210 (Fig. 2 (C)).

The surface of the thus obtained aluminum electrode is anodically oxidized thereafter to form an oxide layer 211 on the surface thereof. The process of anodic oxidation is effected in an ethylene glycol solution containing from 1 to 5% of tartaric acid. Thus is obtained a 2,000 Å thick oxide layer 211 on the surface of the aluminum electrode. Because the thickness of the oxide layer 211 thus obtained corresponds to the length of the offset gate region that is formed in the later step of ion doping, the

length of the offset gate region can be determined in this step of anodic oxidation (Fig. 2 (D)).

Then, by means of ion doping process (also known as plasma doping process), an impurity (phosphorus) for rendering the portion N-conductive is added into the active layer region (which constitutes source/drain and a channel) in a self-aligned manner using the gate electrode portion, i.e., the gate electrode 210 and the surrounding oxide layer 211. In the present example, phosphine (PH_3) is introduced as the doping gas to implant phosphorus at a dose in a range of from 1×10^{15} to 8×10^{15} cm^{-2}, for example, at a dose of 4×10^{15} cm^{-2} by applying an accelerating voltage of from 60 to 90 kV, for example, at 80 kV. N-type impurity regions 212 and 213 are formed as a result. It can be seen from the figure that the impurity region is formed offset from the gate electrode for a distance of x. Such an offset structure is effective, because the leak current (sometimes referred to as an "off current"), which is observed when a reversed voltage (i.e., a negative value in case of an N-channel TFT) is applied to the gate electrode, can be effectively lowered. Particularly in a TFT for use in the control of a pixel electrode as in the present example, the leak current is preferably as low as possible. By lowering the leak current, the charge can be accumulated in the pixel electrode to reproduce favorable images.

Annealing is effected by irradiating a laser beam using a KrF excimer laser (operating at a wavelength of 248 nm and a pulse width of 20 nsec). The laser is operated to provide from 2 to 10 shots per site, for example, 2 shots per site, at an energy density of from 200 to 400 mJ/cm^2, for instance, at 250 mJ/cm^2. Furthermore, a more effective annealing can be realized by heating the substrate in a range of from about 200 to 450°C (Fig. 2 (E)).

Then, a 6,000 Å thick silicon oxide film 214 is deposited as an interlayer insulating layer by means of plasma CVD. Furthermore, a transparent polyimide film 215 is formed thereon by spin coating to obtain a planarized surface. A 800 Å thick clear conductive film (an ITO film) is deposited By sputtering on the thus obtained planarized surface, and is patterned to provide a pixel electrode 216.

Contact holes are formed in the interlayer insulating layers 214 and 215. Thus, electrode and interconnection 217 and 218 are formed by using film comprising titanium nitride and aluminum. Finally, a pixel circuit having a TFT for an active matrix device is obtained by annealing the resulting structure at 350°C for a duration of 30 minutes under gaseous hydrogen at 1 atm.

As described above, the method according to the present invention provides a high performance semiconductor device with high productivity by using a crystalline silicon film which is obtained by a rapid and low temperature crystallization process. This rapid and low temperature crystallization is realized by selectively introducing a catalyst element using a resist.

In the example above, a layer containing a catalyst was formed on the surface of the substrate by applying a solution containing the catalyst. However, it should be noted that it is also in the scope of the present invention a method which comprises forming previously a layer containing the catalyst on the substrate, and then depositing thereon an amorphous silicon film.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed on said second insulating film.

2. A semiconductor device of claim 1 wherein said semiconductor layer comprises crystalline silicon.

3. A semiconductor device of claim 1 wherein said first insulating film comprises silicon oxide.

4. A semiconductor device of claim 1 wherein said second insulating film comprises polyimide.

5. A semiconductor device of claim 1 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

6. A semiconductor device of claim 1 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

7. A semiconductor device of claim 1 wherein a portion of said pixel electrode is under said electrode.

8. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed on said second insulating film.

9. A semiconductor device of claim 8 wherein said semiconductor layer comprises crystalline silicon.

10. A semiconductor device of claim 8 wherein said first insulating film comprises silicon oxide.

11. A semiconductor device of claim 8 wherein said second insulating film comprises polyimide.

12. A semiconductor device of claim 8 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

13. A semiconductor device of claim 8 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

14. A semiconductor device of claim 8 wherein a portion of said pixel electrode is under said electrode.

15. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed on said second insulating film.

16. A semiconductor device of claim 15 wherein said semiconductor layer comprises crystalline silicon.

17. A semiconductor device of claim 15 wherein said first insulating film comprises silicon oxide.

18. A semiconductor device of claim 15 wherein said second insulating film comprises polyimide.

19. A semiconductor device of claim 15 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

20. A semiconductor device of claim 15 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

21. A semiconductor device of claim 15 wherein a portion of said pixel electrode is under said electrode.

22. A semiconductor device of claim 15 wherein said transparent pixel electrode comprises indium tin oxide.

23. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed on said second insulating film

24. A semiconductor device of claim 23 wherein said semiconductor layer comprises crystalline silicon.

25. A semiconductor device of claim 23 wherein said first insulating film comprises silicon oxide.

26. A semiconductor device of claim 23 wherein said second insulating film comprises polyimide.

27. A semiconductor device of claim 23 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

28. A semiconductor device of claim 23 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

29. A semiconductor device of claim 23 wherein a portion of said pixel electrode is under said electrode.

30. A semiconductor device of claim 23 wherein said transparent electrode comprises indium tin oxide.

31. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate

structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a pixel electrode formed on said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode wherein said second conductive film is interposed between said pixel electrode and said first conductive film; and

a conductive layer formed on said second insulating film and connected to the other one of said first and second impurity regions.

32. A semiconductor device of claim 31 wherein said semiconductor layer comprises crystalline silicon.

33. A semiconductor device of claim 31 wherein said first insulating film comprises silicon oxide.

34. A semiconductor device of claim 31 wherein said second insulating film comprises polyimide.

35. A semiconductor device of claim 31 wherein said second conductive film comprises titanium nitride.

36. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed on said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode wherein said second conductive film is interposed between said pixel electrode and said first conductive film; and

a conductive layer formed on said second insulating film and connected to the other one of said first and second impurity regions.

37. A semiconductor device of claim 36 wherein said semiconductor layer comprises crystalline silicon.

38. A semiconductor device of claim 36 wherein said first insulating film comprises silicon oxide.

39. A semiconductor device of claim 36 wherein said second insulating film comprises polyimide.

40. A semiconductor device of claim 36 wherein said second conductive film comprises titanium nitride.

41. A semiconductor device of claim 36 wherein said transparent pixel electrode comprises indium tin oxide.

42. A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel formation region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed on said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed on said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode wherein said second conductive film is in direct contact with said one of the impurity regions and said transparent pixel electrode and said first conductive film is formed on said second conductive film; and

a conductive layer formed on said second insulating film and connected to the other one of said first and second impurity regions, wherein said electrode comprises a same material as said conductive layer.

43. A semiconductor device of claim 42 wherein said semiconductor layer comprises crystalline silicon.

44. A semiconductor device of claim 42 wherein said first insulating film comprises silicon oxide.

45. A semiconductor device of claim 42 wherein said second insulating film comprises polyimide.

46. A semiconductor device of claim 42 wherein said second conductive film comprises titanium nitride.

47. A semiconductor device of claim 42 wherein said transparent pixel electrode comprises indium tin oxide.

ABSTRACT

In a method for crystallizing an amorphous silicon film by a heat treatment that is effected for a duration of about 4 hours at about 550°C using a catalyst element for accelerating the crystallization, the quantity of the catalyst element to be introduced into the amorphous silicon is precisely controlled. A resist mask 21 is formed on the surface of an amorphous silicon film 12 provided on a glass substrate 11, and an aqueous solution 14, e.g., an acetate solution, containing a catalyst element such as nickel at a concentration controlled in a range of from 10 to 200 ppm (need to be adjusted) is supplied dropwise thereto. After maintaining the state for a predetermined duration of time, the entire substrate is subjected to spin drying using a spinner 15. A thin film of crystalline silicon is finally obtained by applying heat treatment at 550°C for a duration of 4 hours.

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【書類名】 図　面

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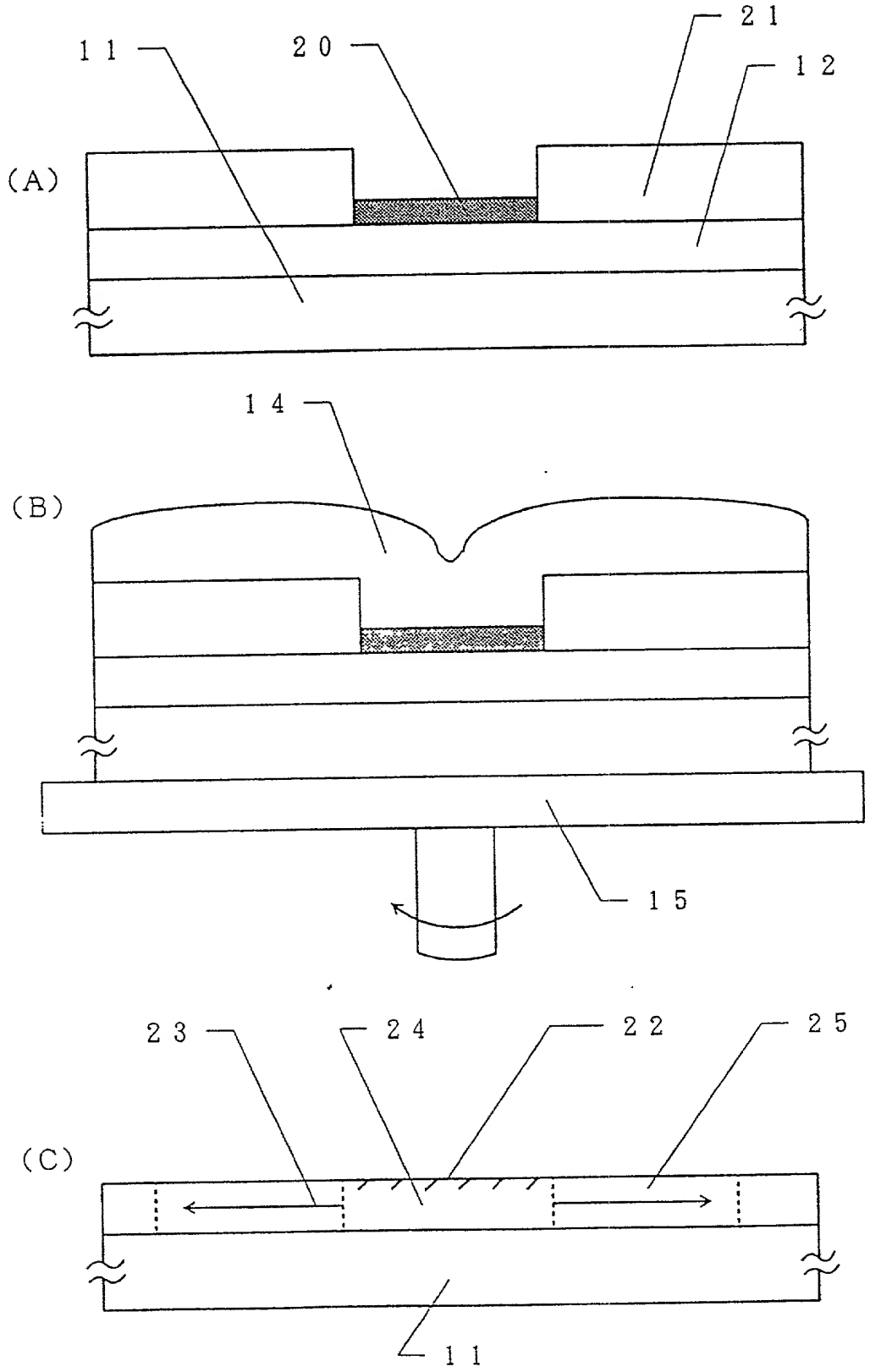

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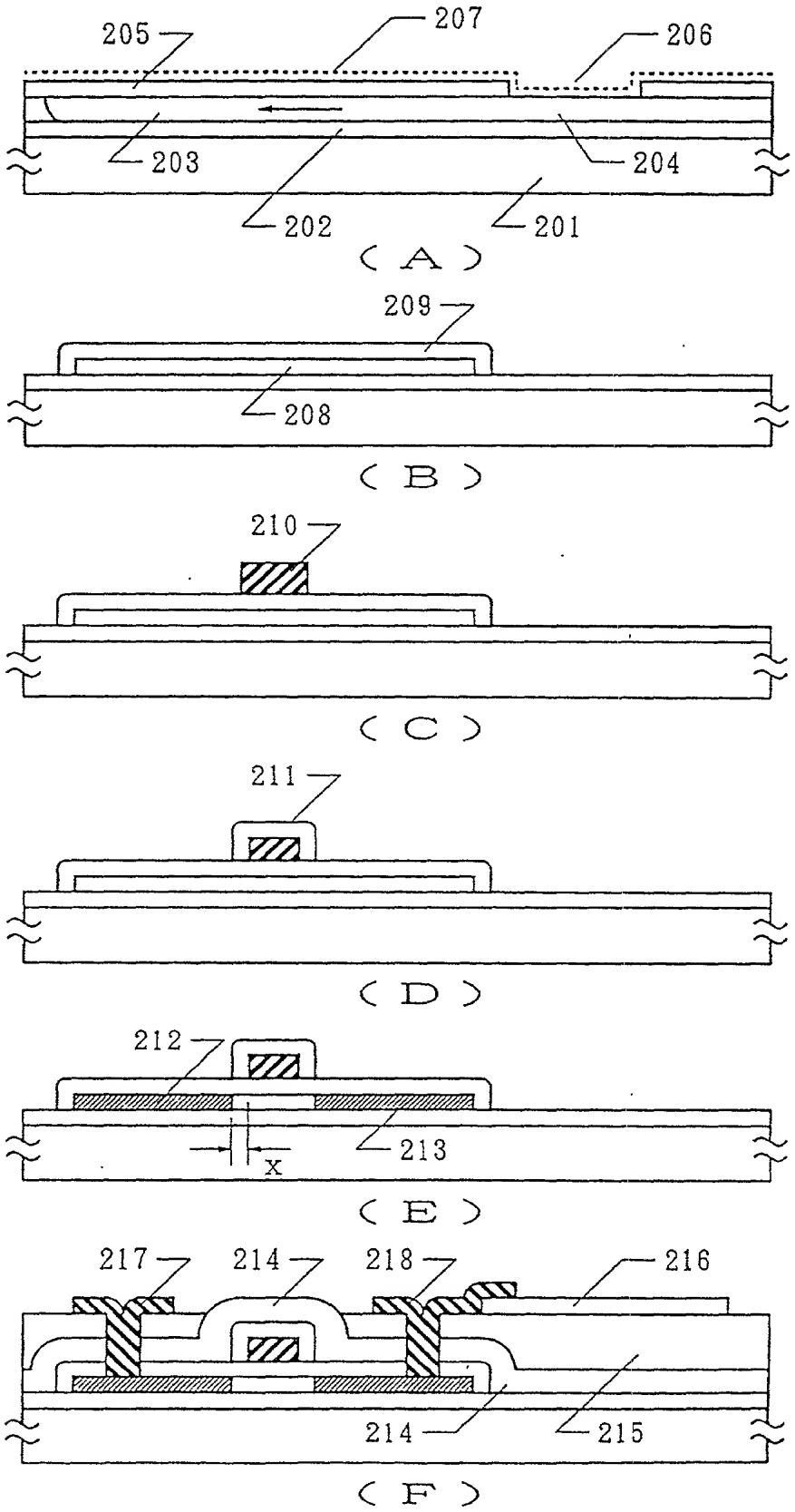
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DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

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PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

* Insert Title

_____, the specification of which is attached hereto unless the following box is checked:

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☐ The specification was filed on _____
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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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Prior Foreign Application(s)

Priority Claimed

Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed	
5-339399	JAPAN	December 2, 1993	☒ Yes	☐ No
			☐ Yes	☐ No
			☐ Yes	☐ No
			☐ Yes	☐ No
			☐ Yes	☐ No

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

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I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)	Gerald J. Ferguson, Jr. (Reg. No. 23,016)
Stuart J. Friedman (Reg. No. 24,312)	David S. Safran (Reg. No. 27,997)
Charles M. Leedom, Jr. (Reg. No. 26,477)	Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Insert Full Name of First or Sole Inventor and Date This Document Is Signed ➡

FULL NAME OF SOLE OR FIRST INVENTOR Hisashi OHTANI	INVENTOR'S SIGNATURE 大谷 久	DATE 94/11/14
RESIDENCE (City, State & Country) Kanagawa, Japan		CITIZENSHIP Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country) Mac Aikoishida Court 501 7-896-1, Takamori, Isehara-shi, Kanagawa-ken 259-11 Japan		
Second Inventor: see above FULL NAME OF SECOND JOINT INVENTOR, IF ANY Hiroki ADACHI	INVENTOR'S SIGNATURE 安達宏樹	DATE 94/11/14
RESIDENCE (City, State & Country) Kanagawa, Japan		CITIZENSHIP Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country) Flat SEL-B 206, 304-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan		
Third Inventor: see above FULL NAME OF THIRD JOINT INVENTOR, IF ANY Akiharu MIYANAGA	INVENTOR'S SIGNATURE Akiharu Miyanaga	DATE 94/11/15
RESIDENCE (City, State & Country) Kanagawa, Japan		CITIZENSHIP Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country) 2-505, 3-4-1, Minamigaoka, Hadano-shi, Kanagawa-ken 257 Japan		
Fourth Inventor: see above FULL NAME OF FOURTH JOINT INVENTOR, IF ANY Toru TAKAYAMA	INVENTOR'S SIGNATURE Toru Takayama	DATE 94/11/14
RESIDENCE (City, State & Country) Kanagawa, Japan		CITIZENSHIP Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country) 1-1104, 1-16-1, Kamoi, Midori-ku, Yokohama-shi, Kanagawa-ken 226 Japan		

Docket No. 0756-2149

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Hisashi OHTANI et al.	)
Based On Serial No. 08/861,001	) Art Unit: 2824
Which Was Filed: May 21, 1997	) Examiner: M. Lebentritt
For: METHOD FOR MANUFACTURING	)
A SEMICONDUCTOR DEVICE	) Date: June 14, 2000

NOTICE OF CHANGE OF COMPANY NAME AND ADDRESS

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Effective immediately, please note that the company name and address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102

Telephone (703) 790-9110

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

Nixon Peabody LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110